APPLICATION NO. 10663705

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CLMPTO

1. A semiconductor device comprising:

a gate electrode formed on semiconductor substrate with an insulation film formed therebetween;

a source region formed on one side of the gate electrode and having a lightly doped source region and a heavily doped source region having a higher carrier concentration than the lightly doped source region;

a drain region formed on the other side of the gate electrode and having a lightly doped drain region and a heavily doped drain region having a higher carrier concentration than the lightly doped drain region;

a first silicide layer formed on the source region;

a second silicide layer formed on the drain region;

a first conductor plug connected to the first silicide layer; and

a second conductor plug connected to the second silicide layer,

the heavily doped drain region being formed in a region of the lightly doped drain region except a peripheral part thereof, and

the second silicide layer being formed in a region of the heavily doped drain region except a peripheral part thereof.

2. A semiconductor device according to claim 1, wherein

the second conductor plug is formed down to a part of the second silicide layer except a peripheral part thereof.

3. A semiconductor device according to claim 1, wherein

a distance between the edge of the heavily doped drain region on the side of the gate electrode and the edge of the lightly doped drain region on the side of the gate electrode is larger than a distance between the edge of the heavily doped source region on the side of the gate electrode and the edge of the lightly doped source region on the side of the gate

electrode.

4. A semiconductor device according to claim 1, wherein

a distance between the edge of the second silicide layer on the side of the gate electrode and the edge of the heavily doped drain region on the side of the gate electrode is larger than a distance between the edge of the first silicide layer on the side of the gate electrode and the edge of the heavily doped source region on the side of the gate electrode.

5. A semiconductor device according to claim 1, wherein

the heavily doped source region is formed also at a part of the peripheral part of the lightly doped source region.

6. A semiconductor device according to claim 1, wherein

the first silicide layer is formed also at a part of the peripheral part of the lightly doped source region.

7. A semiconductor device according to claim 1, wherein

the first conductor plug is formed down to a region of the first silicide layer except a peripheral part thereof.

8. A semiconductor device according to claim 1, further comprising another insulation film formed on the peripheral part of the lightly doped drain region and the peripheral part of the heavily doped drain region, and

in which the second silicide layer is formed in a region of the heavily doped drain region where the said another insulation film is not formed.

9. A semiconductor device according to claim 8, further comprising a sidewall insulation film formed on the side wall of the gate electrode, and

in which said another insulation film is formed also on the side wall of the sidewall insulation film.

10. A semiconductor device according to claim 1, wherein

the distance between the edge of the second silicide layer and the edge of the heavily doped drain region is 0.1 μm or above.

11. A semiconductor device according to claim 10, wherein

the distance between the edge of the second silicide layer and the edge of the heavily doped drain region is 0.5 μm or above.

12. A semiconductor device according to claim 1, further comprising an element isolation region adjacent to the drain region, and

in which the heavily doped drain region is spaced from the element isolation region.

13. A semiconductor device according to claim 12, wherein

the heavily doped source region is in contact with the element isolation region.

14. A semiconductor device according to claim 12, wherein

the first silicide layer is in contact with the element isolation region.

15. A semiconductor device according to claim 1, wherein

the distance between the edge of the conductor plug and the edge of the second silicide layer is 0.3 μm or above.

16. A semiconductor device according to claim 1, further comprising a third silicide layer formed on the gate electrode.

CLAIMS 17-20 (CANCELLED)